UNITED TELECOMS LIMITED

Technical Datasheet

Model No: UTL-MP-0072-1RU

LXMR

(4 X 10G MUXPONDER)

Version: 01

Released on: January 13, 2026

UNITED TELECOMS LIMITED

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Chapter 1

LXMR: System Introduction

1. Introduction

1.1 Objective and Background

This document's objective is to offer the reader a comprehensive view of the technical specifications of the LXMR (4 X 10G Muxponder) system. It covers essential details about the system's technical parameters and features.

1.2 Scope

This 40G Muxponder card can be used in DWDM and Optical Transport Network (OTN) systems for aggregating and multiplexing low-bit-rate clients (up to 2.5G) as well as for transponder applications. 16 client ports, along with 4-line ports, have been provided on the face plate of the LXMR card. LXMR can be housed in a standard 19-inch DWDM Sub rack, 23-inch 12T OTN rack, or in a pizza box configuration for a standalone application.

The 40G MUXPONDER board provides 16 multi-rate client interfaces (STM1/4/16/64, 1GE/10GE, OTU1,2 rate), four 10G line-side OTU2 interfaces with a maximum bandwidth of 40Gbps, one Ethernet interface (available for standalone debug and FTP), and one USB (TYPE-B) interface for debugging. Each card supports two 10/100/1000 Mbps Ethernet PHY interfaces to support the control path through the backplane/pizza box rear side.

1.3 System Introduction

Figure 1: LXMR (pizza box)

The **UTL**-40G Muxponder Solution comprising of 16 SFP ports which can be configured to Ethernet, Fibre Channel (FC), Synchronous Optical Network (SONET), Synchronous Digital Hierarchy (SDH), Common public Radio Interface (CPRI), Optical Transport Unit (OTU2) and maps them into 4X10G SFP+ based pluggable line optics with a max throughput of 10G.

The Solution provisions protection that extends to both the line and the client side. It operates flexibly in 6 and 14-slot chassis as well as a standalone 1U pizza box.

Possible ports combination:

LXMR ports:

- 16 X 1G/2.5G → 4 X OTU2
- 12 X 1G/2.5G + 1 X 10GbE → 4 X OTU2
- 8 X 1G/2.5G + 2 X 10GbE → 4 X OTU2
- 4 X 1G/2.5G + 3 X 10GbE → 4 X OTU2
- 4 X 10GbE → 4 X OTU2

1.4 References

1. ITU-T Recommendation G.709 - Interfaces for the Optical Transport Network.
2. Process document for Functional Specification and Unit Testing.
3. Datasheets of the devices used on the LXMR board.
4. Generic Requirements for 40/80 Channel DWDM Equipment with Channel Bit rates up to 40Gbps for Core Network Application (TEC/GR/TX/WDM-007/09/MAR-2016).

Chapter 2

Functional specifications

2. LXMR: Block Level description

There are 16 client ports (low rate, 1G/2.5G) on the face plate and 4 line ports (10G for OTU2) on the face plate. 4 out of the 16 client ports are 10G capable. These 16 clients are connected to the client side of the OTN processor, while four of the line ports are going to the SFP+ on board.

The OTN processor offers termination, processing, framing, multiplexing, demultiplexing, and switching of OTN signals, in addition to client-side mapping of SONET/SDH and Ethernet signals to OTN signals. OTN processors' HPI interface provides configuration and monitoring support, and

it is getting connected to a dedicated FPGA for the OTN processor. The FPGA also provides an overhead interface connection to the OTN processor and can be used for the insertion and extraction of overhead from OTN containers. CPLD is acting as a bridge to communicate between the FPGA and the control processor.

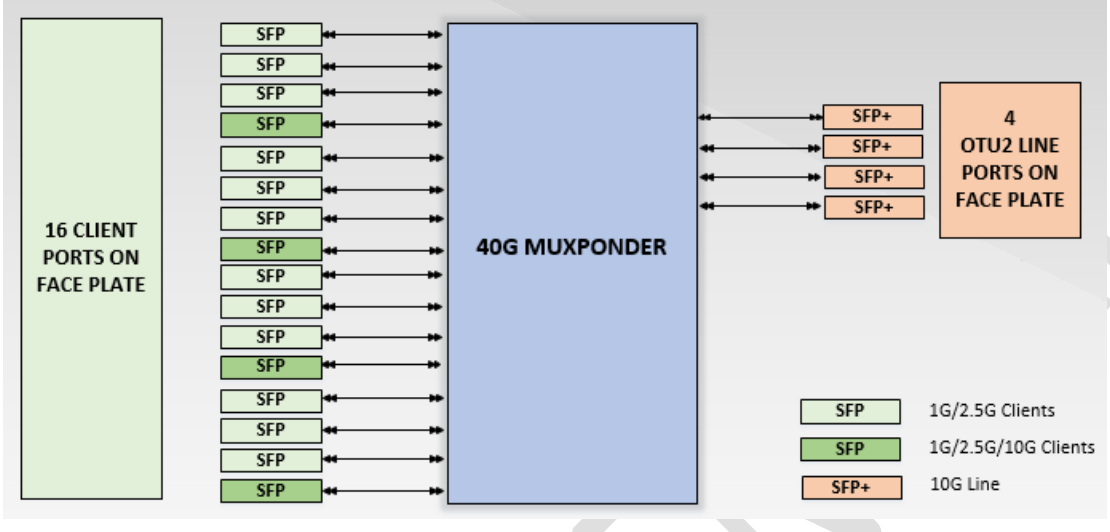

Figure 2: Datapath configuration (4 x10G)

The solution is designed with the latest OTN standards and supports ODUk-based encapsulation for efficient use of network bandwidth; it supports configuration to be done remotely or through the Element Management System (EMS).

To cater to the demand for increasing data capacity, the mobile operators are relying on reduced OPEX attributed to the cell. Typical application of the system is depicted in Figure 1 below.

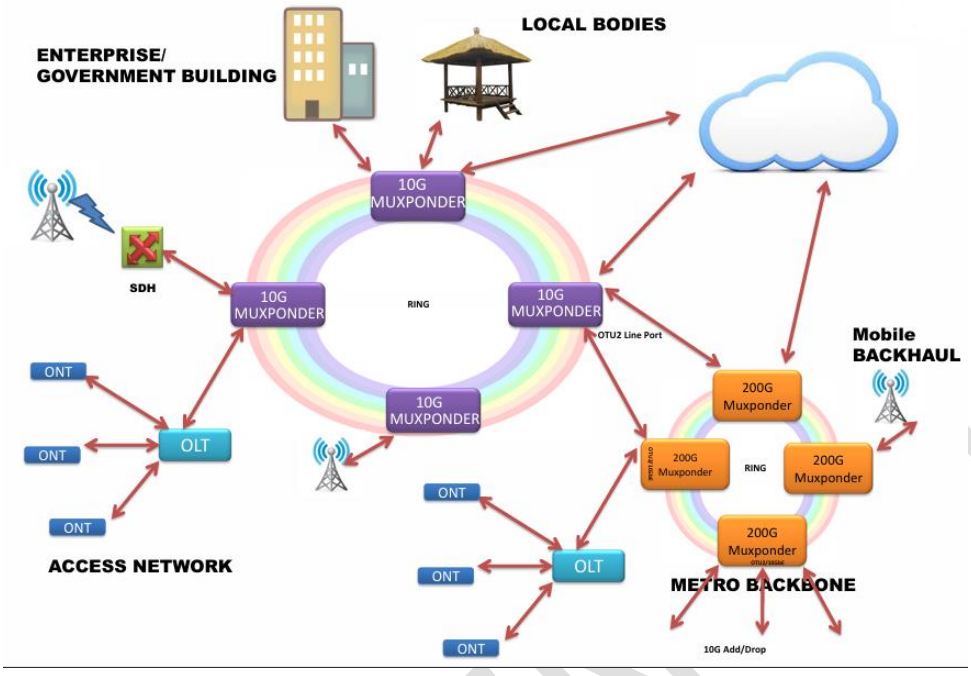

Figure1: Application

2.1 FUNCTIONAL BLOCKS

Functionally 40G Muxponder Card is divided into the following blocks:

1. Power Supply Block
2. Programmable Logic Devices Block
3. Data path Block
4. Processor Block

2.1.1 Power Supply Block

Input: -48 V DC@4A (-40V to -60V DC)

2.1.1.1 Power Entry Module

It has dual, hot-swap 48V dc power inputs and also provides EMI filtering. Besides processing the main –48V bus (coming from the chassis), the module also provides a completely isolated auxiliary 3.3V to PSOC and CSOC.

The main functionality of the module is to provide -48V Dual Feeds OR 'Ing, inrush protection for hot swap capability and EMI filtering to attenuate the noise generated by the downstream DC/DC converters.

2.1.1.2 Isolated (-48V to 12V) DC-DC Converter

It is an isolated dc-dc converter that operates over an input voltage range from -36 V to -75 V DC and provides a single regulated output.

This DC/DC power module is used to provide a 12V DC intermediate bus from –48V coming from the shelf. This 12V is used to generate multiple low voltages through discrete/modular point of load (POL) converters.
Another isolated DC-DC converter is used for the generation of 12V for fans used in the Standalone Pizza Box configuration.

2.1.1.3 Non-Isolated DC-DC Converters

Apart from the power supply for the power entry module and two types of isolated DC-DC power modules, two types of non-isolated DC-DC converter and three LDO Regulators, based on the output current requirement, have been used

2.1.2 Programmable Logic Devices Block

For various interrupt handling, SFP+/SFP status accessibility to the processor, configurability of Control Processor, Achieving Devices Reset timing constraints, Power Good monitoring of the DDR Power Supply and of the Hot Swap Controller, to provide necessary hardware for LED ON/OFF or Blinking, and some logic; PSOC, CSOC, and CPLD and FPGA have been used.
CPLD and FPGA are separately interfaced to the processor through the local bus interface of the processor, enabling the processor to access the registers created inside them.

2.1.3 Data Path Block

The Data Path section mainly consists of the following sub-sections.

2.1.3.1 OTN Processor

- The OTN processor offers termination, processing, framing, multiplexing, demultiplexing, and switching of OTN signals, in addition to client-side mapping of SONET/SDH and Ethernet signals to OTN signals.
- OTN Processor needs 155.52 MHz clock +/-20ppm for its timing requirements. The OTN processor generates all the other required clocks internally.
- This device also has a generic host interface used in HPI (host processor interface) mode to connect with the CPLD as a bridge to map the processor commands. So, overall control processor of the card is communicating with the OTN processor.
- The OTN processor also has an External Overhead Interface, which can provide overhead data to an external device or can take overheads from an external device and put them in OTN overheads

2.1.3.2 Client Optics

- There are 16 SFP modules on board for client interface. These SFP modules interface directly to the OTN processor client side.
- The static signals to the SFP+ are managed by the control processor through the CPLD. Besides this, the I2C bus is used to manage 16 SFP from the onboard control processor.

2.1.3.3 Line Optics

- Line optics contain 4 SFP+ mounted in two pairs and are connected to the OTN processor line side.
- The static signals to the SFP+ are managed by the control processor through the CPLD. Besides this, the I2C bus is used to manage 4 SFP+ from the onboard control processor.

2.1.3.4 Processor Block

This block consists of a DUAL CORE QORIQ integrated communications processor, which interfaces and controls all the components of the LXMR and provides control information to the SCMs via the dedicated base channel.

The MDC/MDIO interface of the processor (master) acts as the management interface, is taken to QUAD PHY and to single port debug PHY in clause 22 mode.

Chapter 3

System Features

3. Salient Features

- Available in two formats:
  - 1U Pizza box for standalone applications
  - Chassis-Based Solution
- Client as well as line 1:1 protection
- Numerous protocols compatible at both client and line side
- Synchronization of the system through the network clock
- Low power consumption
- Remote configuration and management.
- Management of the entire system through LCT/EMS

Chapter 4

Technical Parameters

*** SFP optical parameters may change based on pluggable unit used during deployment.**

**** UTL may make changes at any time to the products or specifications contained herein as per requirement.**

System Requirements	Can be housed in 6U and 14U chassis. It can also operate as a standalone 1U pizza box.
Port Format Client-side Interfaces Line-side Interfaces	 FE/GbE/CBR2G5/10GE FC-100/FC-200/FC-400/FC-800/ FC-1200 SONET OC-3/OC-12/OC-48/OC-192 SDH STM-1/STM-4/STM-16/STM-64 OTN OTU0/OTU1/OTU2/OTU2e OTU2 OTU2e OTU1
Power Requirements (with optics)	Chassis mode: 130W (Max) Pizza box mode: 150W (Max),100W (Typical)
Optical Power Budget	
Client Side SFP Ports	Tx (-5 to 0dBm) , Rx Input power max – 3 dBm , Rx Sensitivity @1.25G (-19dBm) Link distance 20km over SM fiber
Line Interface SFP + Ports	Tx (-4 to +0.5dBm), Rx Input power max + 0.5 dBm , Rx Sensitivity @10G (-15 dBm) Link distance 20km over SM fiber
Protection	1+1 Line Protection 1:1 Per Port Client Protection via Protection Card
FEC Modes	Standard G.709 GFEC for all OTU0/1/2 signals. Enhanced (ITU-T G.975.1 I.4) and Ultra (ITU-T G.975.1 I.7) FEC for network side OTU2 signals
Environmental Conditions Operating Temperature Relative Humidity	 -0°C to +40°C 5% to 95% (non-condensing)
Physical Characteristics	CHASSIS mode - 322.25 mm (H) X 280 mm (W) X 34.3 mm (D) PIZZA BOX – 446 mm (H) X 320 mm(W) X 43.7 mm(D)

4. Technical Parameters

Annexure – I

Abbreviations

A. Acronyms

OTN	Optical Transport Network
LXMR:	40G Muxponder Card.
DWDM:	Dense Wavelength Division Multiplexing
GPIO:	General Purpose Input Output.
OCN:	Optical Core Network
EMS:	Element Management System.
LCT:	Layered Coding Transport